



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/997,019	11/28/2001	John Whitman	4294.2US (98-1208.2)	6139
24247	7590	10/19/2004	EXAMINER	
TRASK BRITT P.O. BOX 2550 SALT LAKE CITY, UT 84110			KEBEDE, BROOK	
			ART UNIT	PAPER NUMBER
			2823	

DATE MAILED: 10/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.



UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

MAILED

OCT 19 2004

GROUP 2800

Application Number: 09/997,019
Filing Date: November 28, 2001
Appellant(s): WHITMAN ET AL.

Brick G. Power
For Appellant

This is in response to the appeal brief filed August 19, 2004.

(1) *Real Party in Interest*

A statement identifying the real party in interest is contained in the brief.

(2) *Related Appeals and Interferences*

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) *Status of Claims*

The statement of the status of the claims contained in the brief is correct.

(4) *Status of Amendments After Final*

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) *Summary of Invention*

The summary of invention contained in the brief is correct.

(6) *Issues*

The appellant's statement of the issues in the brief is correct.

(7) *Grouping of Claims*

The appellants' statement in the brief that certain claims do not stand or fall together is not agreed with because of the following reasons:

Appellants, in one hand, state that claims 1, 2, 6,7, and 10-22 are grouped together and claims 2, 6,7, and 10-22 stand with claim 1. Appellants, on the other hand, state that claims 2, 10, 13 or 15 do not fall with claim 1. These statements are contradictory. In addition, appellants did not provide reasons why claims 2, 10, 13 or 15 do not stand or fall with claim 1. Therefore, claims 2, 10, 13 or 15 should also stand or fall with claim 1.

(8) *Claims Appealed*

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) *Prior Art of Record*

6,461,932	Wang	10-2002
6,228,711	Hsieh	5-2001
6,117,486	Yoshihara	9-2000

(10) *Grounds of Rejection*

The following ground(s) of rejection are applicable to the appealed claims:

a. Claims 1, 2, 6, 7, and 10-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Wang (US/6,461,932).

Re claim 1, Wang discloses a method for preparing a surface of a semiconductor device structure for planarization, comprising: providing a semiconductor device structure (see Fig. 4d) including at least one recess (54) (i.e., trench in the silicon substrate 40) formed in a surface thereof and a first material layer (56) substantially filling the at least one recess (54) and covering the surface (not labeled), the first material layer (56) having a non-planar surface (see Fig. 4d); applying a second material (60) to the first material layer (56); and spreading the second material (60) over the first material layer (56) so as to forming a second material layer (60) having a planar surface (see Col. 6, lines 29-37) without requiring subsequent planarization of the second material (see Fig. 4d).

Re claim 2, as applied to claim 1 above, Wang discloses all the claimed limitations including the limitation wherein the applying said second material comprises applying a stress buffer material to the first material layer (see Fig. 4d).

Re claim 6, as applied to claim 1 above, Wang discloses all the claimed limitations including the limitation wherein said providing comprises providing a shallow trench isolation structure with the at least one recess comprising at least one trench formed in a surface of said shallow trench isolation structure (see Fig. 4d).

Re claim 7, as applied to claim 6 above, Wang discloses all the claimed limitations including the limitation providing the shallow trench isolation structure with the first material layer comprising an electrical insulator material (see Figs. 4d-4g).

Re claim 10, as applied to claim 2 above, Wang discloses all the claimed limitations including the limitation wherein the spreading comprises at least partially filling at least one valley of the first material layer with the stress buffer material while leaving at least one peak of said first material layer substantially uncovered by the stress buffer material (see Figs. 4d and 4e).

Re claim 11, as applied to claim 10 above, Wang discloses all the claimed limitations including the limitation planarizing at least said first material layer (see Figs. 4d and 4e).

Re claim 12, as applied to claim 11 above, Wang discloses all the claimed limitations including the limitation wherein the planarizing comprises etching at least one region of the first material layer exposed through the stress buffer material with selectivity over the stress buffer material (see Figs. 4d and 4e).

Re claim 13, as applied to claim 12 above, Wang discloses all the claimed limitations including the limitation wherein said etching is effected until a surface of the at least one region is in substantially the same plane as a surface of the stress buffer material (see Figs. 4d and 4e).

Re claim 14, as applied to claim 13 above, Wang discloses all the claimed limitations including the limitation wherein the planarizing further comprises abrasively planarizing the

Art Unit: 2823

stress buffer material and the at least one region to expose the surface of said semiconductor device structure adjacent the at least one recess, said surface of the semiconductor device structure and a surface of the first material layer in the at least one recess being located in substantially the same plane following said planarizing (see Figs. 4d and 4e).

Re claim 15, as applied to claim 13 above, Wang discloses all the claimed limitations including the limitation wherein said planarizing further comprises concurrently etching said first material layer and the stress buffer material at substantially the same rate so as to expose said surface of the semiconductor device structure adjacent the at least one recess with the surface of the semiconductor device structure and a surface of said first material layer in the at least one recess being located in substantially the same plane following said planarizing (see Figs. 4d-4f).

Re claim 16, as applied to claim 11 above, Wang discloses all the claimed limitations including the limitation wherein the planarizing is effected until said surface of said semiconductor device structure is exposed through the first material layer (see Figs. 4d-4e).

Re claim 17, as applied to claim 16 above, Wang discloses all the claimed limitations including the limitation wherein the etching is effected until a surface of the first material layer in the at least one recess is in substantially the same plane as the surface of said semiconductor device structure (see Figs. 4d-4f).

Re claim 18, as applied to claim 16 above, Wang discloses all the claimed limitations including the limitation removing the stress buffer material from the semiconductor device structure (see Figs. 4d-4f).

Re claim 19, as applied to claim 2 above, Wang discloses all the claimed limitations including the limitation wherein the spreading comprises forming a substantially planar surface over the semiconductor device structure (see Figs. 4d-4f).

Re claim 20, as applied to claim 19 above, Wang discloses all the claimed limitations including the limitation planarizing at least said first material layer (see Figs. 4d-4f).

Re claim 21, as applied to claim 20 above, Wang discloses all the claimed limitations including the limitation wherein the planarizing comprises substantially concurrently abrasively planarizing the stress buffer material and the first material layer to surface of said semiconductor device expose the device structure adjacent the at last one recess, said surface of the semiconductor device structure and a surface of the first material layer in the at least one recess being located in substantially the same plane following the planarizing (see Figs. 4d-4f).

Re claim 22, as applied to claim 20 above, Wang discloses all the claimed limitations including the limitation wherein the planarizing comprises substantially concurrently etching the first material layer and the stress buffer material at substantially the same rate so as to expose the surface of said semiconductor device structure adjacent the at least one recess with said surface of the semiconductor device structure and a surface of the first material layer in the at least one recess being located in substantially the same plane following said planarizing.

b. Claims 3, 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Wang (US/6,461,932) in view of Yoshihara (US/6,117,486).

Re claims 3-5, as applied to claim 1 above, Wang discloses all the claimed limitations. However, Wang does not disclose decreasing a rate of the spinning while permitting the material to at least partially cure and gradually increasing the rate of the spinning.

Art Unit: 2823

Yoshihara discloses applying the material to the surface of the semiconductor device structure; spinning the semiconductor device structure by both decreasing rate of spinning and, while allowing the material to cure gradually, increasing the rate of spinning; exposing the material to a soft balling temperature; spinning rate of 1000 and 100 rpm (see Figs. 10 and Col. 13, lines 25-44).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of appellants' claimed invention was made to provide a material on the semiconductor wafer at predetermined and uniform thickness (i.e., planar surface) by spinning the semiconductor device structure at both decreasing and increasing rate of spinning while allowing the material to cure gradually as taught by Yoshihara.

c. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Wang (US/6,461,932) in view of Hsich (US/6,228,711).

Re claims 8 and 9, as applied to claim 1 above, Wang discloses all the claimed limitations. However, Wang does not specifically disclose providing dual-damascene structure.

Hsich discloses forming of dual-damascene structure and forming a conductive layer over the dual-damascene structure (see Fig. 3H).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to have provided Wang reference with dual-damascene structure as taught by Hsich because, as well-known in the art, the structure would have increased the device density.

(11) Response to Argument

Appellants' arguments filed on August 19, 2004 have been fully considered but they are not persuasive.

Art Unit: 2823

I.

A.

Pertaining to appellants' argument in Pages 6-12, with respect to claims 1, 6, 7, and 10-22, i.e., "Wang lacks any express or inherent description of spreading a second material layer over a first material layer so as to form a second material layer having a planar surface, as recited in independent claim 1...", it is respectfully submitted that the argument is not commensurate with the scope of the rejected claims. As set forth in Paragraph 10(a) above, Wang '932 teaches all the claimed limitation including the limitation *spreading a second material layer over a first material layer so as to form a second material layer having a planar surface*, as recited in claim 1. In addition, the claimed invention is not distinguishable from Wang '932 disclosure, and appellants do not specify in the claims the type of material that is deposited to form the first material and second material layers. Furthermore, the term "spreading" does not have any special meaning, therefore, the term "spreading" is interpreted according to Merriam-Webster online dictionary as set forth herein below.

Art Unit: 2823

Merriam-Webster Online Dictionary

Thesaurus

4 entries found for **spread**.
To select an entry, click on it.

spread[1,verb]
spreading factor
wide-spreading
seafloor spreading



Main Entry: **¹spread** ♦

Pronunciation: 'spred

Function: *verb*

Inflected Form(s): **spread; spread-ing**

Etymology: Middle English *spreden*, from Old English *-spr[AE]dan*; akin to Old High German *spreiten* to spread

transitive senses

1 a : to open or expand over a larger area

<spread out the map> **b** : to stretch out : **EXTEND**

<spread its wings for flight>

2 a : to distribute over an area <spread

fertilizer> **b** : to distribute over a period or

among a group <spread the work over a few

weeks> **c** : to apply on a surface <spread butter

on bread> **d** (1) : to cover or overlay something

with <spread the cloth on the table> (2)

archaic : to cover completely **e** (1) : to prepare or furnish for dining : **SET** <spread the table>

(2) : **SERVE** <spread the afternoon tea>

In addition, the claims are given their broadest reasonable interpretation in light of the supporting disclosure. See *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Also see *In re Hyatt*, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000) Limitations appearing in the specification but not recited in the claim are not read into the claim. See *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969). Also See *In re Zletz*, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).

Since it is relevant to claim 1, Fig. 7 of instant application is reproduced below for demonstrative purpose.

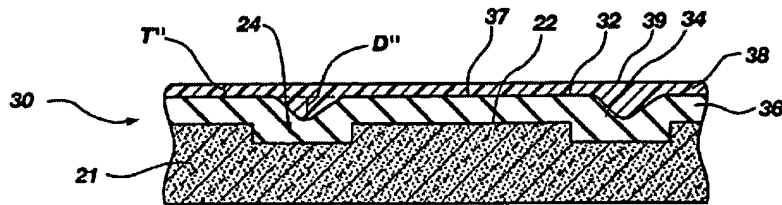
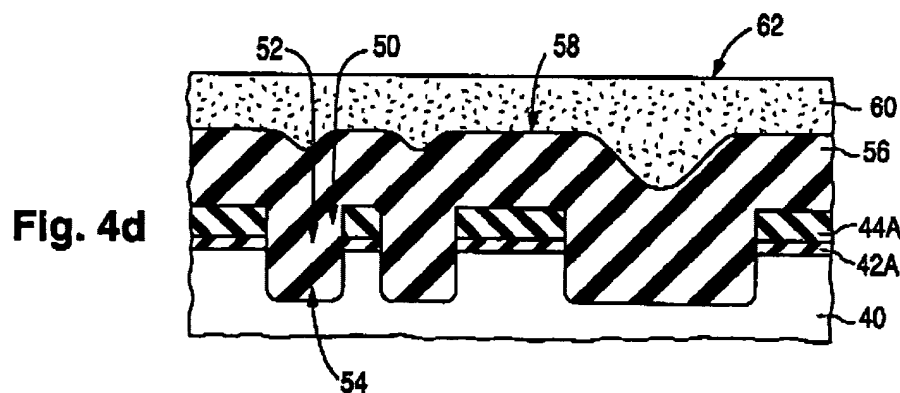


Fig. 7

As depicted above, the first material 36 fills the trenches 24, and the first material 36 has non-planar surface upper surface 37 which includes valleys 34 (see Paragraph 0045 of the instant application). The second material 38 is deposited to fill cover the first layer 36. In addition, the second material 38 is formed by a spin-coating process (see Paragraph 0046 and Paragraphs 0039-0041) to form a planar second material 38 layer as depicted in Fig. 7.

Similarly, Wang '932 discloses a process substantially as claimed, as depicted Fig. 4d below.



As shown in Fig. 4d above, Wang '932 discloses providing a semiconductor device structure including at least one recess 54 (i.e., trench in the silicon substrate 40) formed in a surface thereof and a first material layer 56 (i.e., an insulation layer) substantially filling the at least one recess 54 and covering the surface (not labeled), the first material layer 56 having a

Art Unit: 2823

non-planar surface; applying a second material 60 to the first material layer 56; and spreading the second material 60 (i.e., spin coating process, see Col. 6,) over the first material layer 56 so as to form a second material layer (60) having a planar surface (see Col. 6, lines 29-37) without requiring subsequent planarization of the second material (i.e., no polishing process conducted to planarize second material layer 60). In particular, Wang '932 also disclose that the second material layer 60 can be created by a "deposition/spinning" procedure (i.e., spin-coating process) (see Col. 6, lines 52-64). In addition, as shown above, second material layer 60 has planar surface 62 and which is similar to that of the instant claims.

Wang '932 also disclose the possibility of "slight depression" in the second material layer 60 in the region of the deepest part of the depressed portion upper surface 58 of the first layer 56. (See Wang '932 Col. 6, lines 29-36):

30 Importantly, smoothening layer 60 has an upper surface
62 which is considerably smoother than upper dielectric
surface 58. Ideally, upper smoothening surface 62 is largely
planar. In actuality, there may be slight depressions in upper
smoothening surface 62 at the locations of the deepest parts
35 of the depressed portion of upper dielectric surface 58.
Compared to upper dielectric surface 58, upper smoothening
surface 62 is largely planar.

In addition, Wang '932 disclosure indicates that "largely planar" means planar. Alternatively, because the instant application does not specifically claim that the second material layer 38 is uniformly planar the entire surface of the first material layer 36, the claim reasonably reads on Wang's '932 description that "largely planar" is "planar" surface. In addition, appellants' specification discloses that the second material layer 38 (i.e., stress buffer layer 38) is "substantially planar" (see the instant application specification Page 15, Paragraph 0047). The term "substantially planar" is analogous to "largely planar" as disclosed by Wang '932.

Further, in response to appellants' argument that the drawings of Wang '932 cannot be relied because they are not to scale, appellants' contention is not persuasive because the rejected claims do not contain any measured quantitative dimensional limitation or the degree of planarization. In the absence of specific dimensional limitation in the claims, appellants' contention that Wang's drawing (i.e., Fig. 4d) cannot be relied upon has no merit, and Wang '932 clearly discloses forming the second material layer 60 having planar surface as shown in Fig. 4d above.

With respect to claim 2, appellants also argue that "Wang lacks any expression or inherent description that that the smoothing layer 60 thereof comprises a stress buffer material." Prior to responding to appellants' contention, it is noted that term "stress buffer material" has no special definition. In addition, the rejected claim, i.e., claim 2, does not specifically claim the type of material. See *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). In addition, there is no explicit definition in the specification for "stress buffer layer." See *Sunrace Roots Enter. Co. v. SRAM Corp.*, 336 F.3d 1298, 1302, 67 USPQ2d 1438, 1441 (Fed. Cir. 2003); *Brookhill-Wilk 1, LLC v. Intuitive Surgical, Inc.*, 334 F.3d 1294, 1298 67 USPQ2d 1132, 1136 (Fed. Cir. 2003); *Ferguson Beauregard /Logic Controls v. Mega Systems*, 350 F.3d 1327, 1338, 69 USPQ2d 1001, 1009 (Fed. Cir. 2003).

Since the type of the material is not specified in the rejected claims, the claims are given their plain meaning of "stress buffer." According to Merriam-Webster online dictionary, as set forth below, the term "stress buffer" is presumed to have the ordinary and customary meaning as the material that reduces "shock or damage due to the force pressed body."

Art Unit: 2823

Merriam-Webster Online Dictionary

Thesaurus

11 entries found for **stress**. The first 10 are listed below.

To select an entry, click on it. For more results, [click here](#).

stress[1,noun]
stress[2,transitive verb]
post-traumatic stress disorder
sentence stress
storm and stress
stress fracture



Main Entry: **¹stress**

Pronunciation: 'stres

Function: *noun*

Etymology: Middle English *stresse* stress, distress, short for *destresse* -- more at [DISTRESS](#)

1 : constraining force or influence: as **a** : a force exerted when one body or body part presses on, pulls on, pushes against, or tends to compress or twist another body or body part; *especially* : the intensity of this mutual force commonly expressed in pounds per square inch **b** : the deformation caused in a body by such a force **c** : a physical, chemical, or emotional factor that causes bodily or mental tension and may be a factor in disease causation **d** : a state resulting from a stress; *especially* : one of bodily or mental tension resulting from factors that tend to alter an existent equilibrium **e** : [STRAIN](#), [PRESSURE](#) <the environment is under *stress* to the point of collapse -- Joseph Shoben>

2 : [EMPHASIS](#), [WEIGHT](#) <lay *stress* on a point>

3 *archaic* : intense effort or exertion

4 : intensity of utterance given to a speech sound, syllable, or word producing relative loudness

5 **a** : relative force or prominence of sound in verse **b** : a syllable having relative force or prominence

Merriam-Webster Online Dictionary

Thesaurus

asp entries found for **buffer**.
To select an entry, click on it.

buffer[1,noun]
buffer[2,transitive verb]
buffer[3,noun]
buffer state
buffer zone



Main Entry: **¹buff-er**

Pronunciation: 'b&-f&r

Function: *noun*

Usage: *often attributive*

Etymology: *buff*, v., to react like a soft body when struck

1 : any of various devices or pieces of material for reducing shock or damage due to contact

2 : a means or device used as a cushion against the shock of fluctuations in business or financial activity

3 : something that serves as a protective barrier: as **a** : [BUFFER STATE](#) **b** : a person who shields another especially from annoying routine matters **c** : [MEDIATOR](#) **1**

4 : a substance capable in solution of neutralizing both acids and bases and thereby maintaining the original acidity or basicity of the solution; *also* : a solution containing such a substance

5 : a temporary storage unit (as in a computer); *especially* : one that accepts information at one rate and delivers it at another

- **buff-ered** /-f&rd/ *adjective*

Art Unit: 2823

In this case, “stress buffer layer” is the material used to reduce damage, i.e., to reduce dishing effect, on the first material layer during chemical-mechanical polishing (CMP) process of the first layer in order to form planar shallow trench isolation (see Wang '932 Col. 3, line 1 through Col. 4, line 17).

The claimed invention apparently avoids damage to the insulator layer **36** by providing the stress buffer layer **38** (see the instant application Page 16, Paragraph 0047) during the polishing process. The second material layer **60** (smoothing layer) disclosed by Wang '932, as depicted in Fig. 4d above, is also a stress buffer layer because Wang '932 also avoid damage to the insulating layer during formation of the planar (flat) STI (shallow trench isolation) by CMP process, i.e., the art recognized problem of “dishing.” (See Wang '932 Col. 7, line 15 - Col. 8, line 56).

Therefore, appellants' argument that *Wang lacks any expression or inherent description that that the smoothing layer 60 thereof comprises a stress buffer material* is not persuasive.

With respect to claim 10, appellants argue that “Wang does not expressly or inherently describe” the claimed subject matter recited in claim 10, i.e., wherein spreading comprises at least partially filling at least one valley of the first material layer with the stress buffer material while leaving at least one peak of said first material layer substantially uncovered by the stress buffer material.

According to appellants' own specification, the second material layer (i.e., the stress buffer layer) **38** is deposited on the surface of the first material layer (i.e., insulating layer) **36** by spin-coating process (see the instant application specification Page 8, Paragraph 0018 through Page 9, Paragraph 0022). In order to deposit a material on a surface by the spin-coating process, the material is deposited on the central portion of the surface while the surface is rotated. During

Art Unit: 2823

the spinning operation, the material spreads out over the surface from the center to the periphery of the wafer and this is governed by Newton's first law of motion (i.e., circular motion).

Therefore, initially some of the surface does not receive the coating material, but eventually all the surface is uniformly coated as a result of the spinning operation. This process also is within the scope of Wang '932 disclosure as depicted in Fig. 4d above.

In this regard, appellants' own disclosure does not provide any process that is distinguishable from that of Wang's '932 teachings.

As depicted in Figs. 8 and 9, the instant application shows that the exposed portion of the surface 37 of the first material layer 36 is formed by removing the second material layer 38 after the spin-coating process of Fig. 7. This is also within the scope of Wang '932 disclosure as depicted on Fig. 4e.

Therefore, appellants' argument that Wang '932 does not explicitly or inherently teach the claimed limitation of claim 10 is not persuasive.

In regard to claim 13, appellants argue that "Wang includes no express or inherent description that the dielectric layer 56 may be etched with selectivity over the smoothening layer 60 thereof until a surface of at least one region of the dielectric layer 56 is in substantially the same plane as a surface of the smoothening layer 60..."

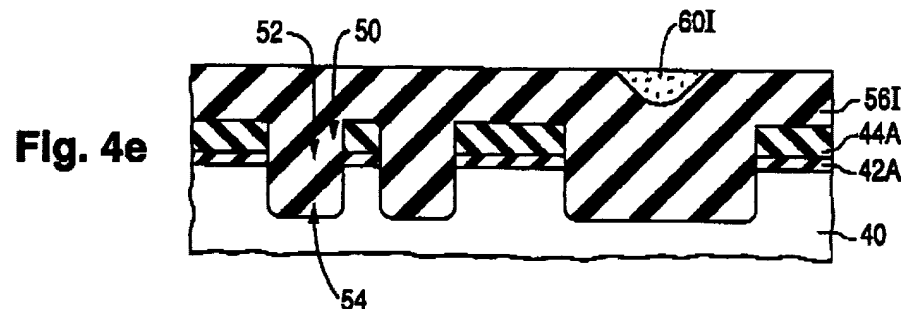
In response to appellants' contention, it is respectfully submitted that appellants' characterization of Wang '932 teaching is not convincing for the following:

Claim 13, which depends from claim 12, recites the limitation "wherein the planarizing comprises etching at least one region of the first material layer exposed through the stress buffer material with selectivity over the stress buffer material; wherein said etching is effected until a

Art Unit: 2823

surface of the at least one region is in substantially the same plane as a surface of the stress buffer material.”

As shown above, there is no particular type of etching process claimed in the rejected claim. The CMP process disclosed by Wang '932 etches some region of the first material layer 56 with selectively over the second material (stress buffer material) 60 until some of the region of the first material 56 becomes planar with the stress buffer material as clearly depicted on Fig. 4e below.



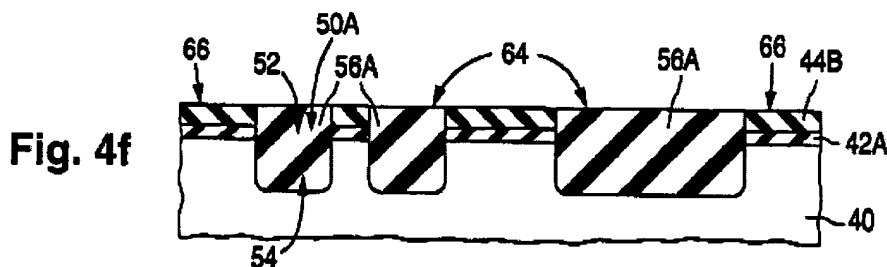
Therefore, appellants' contention that Wang '932 does not explicitly or inherently teach the claimed limitation of claim 13 has no merit.

With respect to claim 15, appellants argue that “Wang includes no express or inherent description that the dielectric layer 56 and the smoothening layer 60 may be etched at substantially the same rate so as to expose a surface of the mask layer 44 adjacent a surface of a portion of the dielectric layer 56 in at least one recess, with the surfaces of the mask layer 44 and the dielectric layer 56 being located in substantially the same plane following such planarization ...”

In response to appellants' argument, it is respectfully submitted that, as explained above for claim 13, appellants do not specifically recited in the claim any particular type of etching process for removing both the first material layer 36 and the second material layer 38. In

Art Unit: 2823

addition, the CMP process of Wang '932, which utilizes chemical and mechanical polishing, is an etching process. As depicted in Fig. 4f below, Wang '932 teaches concurrent etching the first material layer 56I and the second material layer 60I of Fig. 4e (see Fig. 4e in previous page) in order to achieve a planar isolation structure of Fig. 4f as depicted below.



Hence, Wang '932 discloses all the claimed limitations including the limitation wherein said planarizing further comprises concurrently etching said first material layer and the stress buffer material at substantially the same rate so as to expose said surface of the semiconductor device structure adjacent the at least one recess with the surface of the semiconductor device structure and a surface of said first material layer in the at least one recess being located in substantially the same plane following said planarizing. Therefore, appellants' contention that Wang '932 does not explicitly or inherently teach the claimed limitation of claim 15 is not persuasive.

As demonstrated above Wang '932 teaches all the claimed limitations of claims 1, 2, 6, 7, and 10-22 and the rejection under 35 U.S.C. § 102 is deemed proper.

B.

Pertaining to appellants' argument in Pages 13-14, with respect to claims 3-5, i.e., "the Office has not established a prima facie case of obviousness ..."

In response to appellants' argument, it is respectfully submitted that claims 3-5 are not allowable, as demonstrated above, because claim 1 is not allowable. Furthermore, the combination of Wang '932 and Yoshihara '486 would have suggested to one of ordinary skill in the art applying the material to the surface of the semiconductor device structure; spinning the semiconductor device structure; decreasing the rate of spinning, while allowing the material to cure gradually; and finally increasing the rate spinning; exposing the material to a soft balling temperature; spinning the wafer at a rate of 1000 and 100 rpm (see Yoshihara '486 Figs. 10 and Col. 13, lines 25-44).

Both Wang '932 and Yoshihara '486 teachings are directed to coating of material on a substrate for the purpose of fabricating semiconductor device. Therefore, the teachings of Wang '932 and Yoshihara '486 are analogous. It would have been within the scope of ordinary skill in the art to combine the teachings of Wang '932 and Yoshihara '486 in order to modify spin the coating process of Wang '932 by adjusting the spinning rate (rpm) according to the teachings of Yoshihara '486 because one having ordinary skill in the art would have been motivated to look to analogous art teaching alternative spin coating process such as the teachings of Yoshihara '486. In addition, the rationale to combine the references can be found in Yoshihara '486 Col. 13, line 26 - Col. 14, line 67. The strongest rationale for combining references is a recognition, expressly or impliedly in the prior art or drawn from a convincing line of reasoning based on established scientific principles or legal precedent, that some advantage or expected beneficial result would have been produced by their combination. See *In re Sernaker*, 702 F.2d 989, 994-95, 217 USPQ 1, 5-6 (Fed. Cir. 1983).

Therefore, the *prima facie* case of obviousness has been met and the rejection under 35 U.S.C. § 103 is deemed proper.

Art Unit: 2823

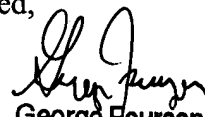
C.

Pertaining to appellants' argument in Page 14-15, with respect to claims 8 and 9, i.e., "claims 8 and 9 are allowable because claim 1 is allowable ...," it is respectfully submitted that claims 8 and 9 should fall with claim 1 for the reasons indicted in Paragraph 11(IA) above. It is respectfully submitted that the combination of Wang '932 and Hsich '711 teach all the limitations of Claims 8 and 9 of the instant application as discussed in Paragraph 10(c) herein above.

Therefore, the *prima facie* case of obviousness burden has been met and the rejection under 35 U.S.C. § 103 is deemed proper.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,


George Fourson
Primary Examiner

Appeal conference has been held on October 7, 2004. The Conferees listed herein below.

1. Olik Chaudhuri, SPE Art Unit 2823 *OC*
2. Wael M. Fahmy, SPE Art Unit 2814 *W.M.F.*
3. George R. Fourson III, Primary Examiner Art Unit 2823 *G*
4. Brook Kebede, Examiner Art Unit 2823 *BK*

BK

October 18, 2004

TRASK BRITT
P.O. BOX 2550
SALT LAKE CITY, UT 84110